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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,213	12/20/2001	Richard Slobodnik	550-298	6125

23117 7590 07/27/2005

NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/022,213	SLOBODNIK, RICHARD	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 7-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4 and 7-11 remain pending in this application. Claims 5, 6, 12 and 14 have been canceled.

2. Applicant states that the subject matter of dependent claims 5 and 7 where incorporated into claim 1, and the subject matter of dependent claims 12 and 14 where incorporated into claim 8. It would appear to the Examiner that claim 7 should be canceled in lieu of the incorporation of this claim into claim 1. **Applicant should cancel claim 7 in reply to this Office Action**.

Response to Arguments

3. Applicant's arguments with respect to claims 1 and 8 have been considered but are moot in view of the new ground(s) of rejection.

4. In response to Applicant's argument on page 6, paragraph 3, that the Examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). The Examiner would also like to point out that Gold's address converter 24

(mapping circuit) would have to be synchronized with the BIST engine 20 as well as embedded memory 28. Gold teaches on page 2, paragraph 17, the address converter 24 can be any conventional type of solid state memory device, such as a read only memory (ROM), a random access memory (RAM), an electronically erasable programmable read only memory (EEPROM), or the like. It would be obvious to on skilled in the art at the time the invention was made that the memories disclosed above are synchronous in their operation and can not function properly if not clocked and synchronized with Gold's BIST engine 20 and embedded memory 28. These arguments presented by the Examiner would also apply to similar argument presented by the Applicant on page 7, paragraphs 2 and 3. The Applicant is also reminded that during patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). See MPEP § 2111.

5. In response to Applicant's argument on page 7, paragraph 1 (top of page), that the references fail to show certain features of Applicant's invention, it is noted that the features upon which applicant relies (i.e., *Gold neither discloses nor suggests that the address remapper could be used to facilitate re-use of the self-test controller with a number of different memories having different mappings between physical memory locations and the logical addresses between these locations as in the present application*) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims.

See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The Examiner would like to point out that in the previous Office Action of Record, paragraph 5, page 5, the Examiner responded to the same argument presented by the Applicant, yet this same argument appears again. The Examiner request that remarks should be directed toward the claim language and not what is in the specification. Furthermore, the language claims 1 and 8 recite that the mapping circuit is "operable to map ...for use by a respective one of said plurality of memories". Even though the claim recites a plurality of memories it appears to the Examiner that the mapping circuit operates on only one memory at a time NOT different memories having different mappings. As it stands the Examiner asserts that Gold still reads on claims 1 and 8 as amended.

6. In response to Applicant's argument on page 8, paragraph 1 (similar to the arguments in paragraph 5 above), that the references fail to show certain features of Applicant's invention, it is noted that the features upon which applicant relies (i.e., *...enabling a generic self-test controller to be adapted for use with a plurality of different memories, each having different logical-to-physical addresses mappings*) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The Applicant further states "a person of ordinary skill in the art would not have been motivated to adapt Gold's system to incorporate further memories, each having an associated mapping circuit". The Examiner asserts that it would have been obvious to one of ordinary skill in the art at the

time the invention was made to duplicate Gold's address converter 24 (mapping circuit) and embedded memory 28 (memory) to make *a plurality of memories each having a mapping circuit*, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8 (7th Cir. 1977).

7. The Applicant's arguments on page 9, paragraph 1, are similar in content as previous arguments outlined above and have been properly responded to by the Examiner.

8. It is the Examiner's conclusion that independent claims 1 and 8 are not patentably distinct or non-obvious over the prior arts of record namely, Gold (US-2003/0167428). Therefore, the rejections are maintained. Based on their dependency on independent claims 1 and 8, claims 2-4, 7, and 8-11, respectively, stand rejected.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-4 and 7-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1:

This claim recites the limitation "a mapping circuit for each of said plurality of memories, said mapping circuit being operable to map...for use by a respective one of said plurality of memories". This renders the claim to be indefinite. It would appear to the Examiner that if there is a mapping circuit per memory then it should not be "said mapping circuit that is operable....for use by a respective one", but "a respective one of said mapping circuits that is operable....for use by a respective one". Correction or further explanation is required.

Claims 1, 4 and 10:

These claims recite the limitation "said at least one memory". There is insufficient antecedent basis for this limitation in the claim. For reason of examination the Examiner is reading this limitation as "said respective one of said plurality of memories".

Claims 7:

This claim is not clear and does not appear to further limit claims 1.

Claim 8:

This claim recites the limitation "the processor core, said plurality of memories, and said self test controller are formed together on an integrated circuit". This is inconsistent with apparatus claim 1, which discloses "said respective one of said plurality of memories" (post 112, 2nd correction). This renders the claim to be indefinite.

This claim recites the limitation "wherein values and timings of signals passed to each of said plurality of memories are adapted to accommodate differing value and timing properties of the respective one of said plurality of memories". This renders the claim to be indefinite. It is not clear to the Examiner why the values passed to the plurality of memories would be adapted to accommodate one of them. This is also not consistent with the apparatus claim 1 which discloses "said interface circuit being operable to adapt values and timings of signals passed between said self-test controller and said respective one of said plurality of memories to accommodate differing value and timing properties of said respective one of said plurality of memories. For reason of examination the Examiner is reading "each of said plurality of memories" as "said respective one of said plurality of memories".

Claim 11:

This claim recites the limitation "said memory". There is insufficient antecedent basis for this limitation in the claim. For reason of examination the Examiner is reading this limitation as "said respective one of said plurality of memories".

Claims 2, 3 and 9:

These claims are also rejected because they depend on claim 1 and 8 and have the same problems of indefiniteness insufficient antecedent basis.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 3, 4, 7, 8, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gold (US-2003/0167428).

Claims 1 and 8:

Gold teaches electronic device 10 includes a BIST engine 20 (self-test controller) that generates a test vector for a physical memory row address of the embedded memory 28 (respective one of said plurality of memories). Gold also teaches a memory address converter 24 Mapping circuit) that converts the physical address generated by the BIST engine 20 to a corresponding logical address in the embedded memory 28. (Page 2, ¶ 17). Gold further teaches an integrated circuit that contains a memory array (respective one of said plurality of memories) and a test generator (controller) coupled to the memory array to generate a physical address of the memory array and a corresponding test vector. (Page 1, ¶ 10). Gold further discloses the microprocessor (processor core) performs BIST on a memory array (respective one of said plurality of memories) having a physical address map distinct from its logical address map. (Page 2, ¶ 16). Gold does not explicitly teach "said mapping circuit is part of an interface circuit", however, Gold does suggest the address converter 24 (mapping circuit) may be adapted to support built-in self-repair of the embedded memory array 28 (respective

one of said plurality of memories). (Page 2, ¶ 21). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Gold's address converter 24 (mapping circuit), in being adapted to support built-in self-repair of the embedded memory array 28 would contain the necessary circuitry to synchronize the timing of the signals connected to the memory array 28. Also, Gold's address converter 24 (mapping circuit) would have to be synchronized with the BIST engine 20 as well as embedded memory 28. Gold teaches on page 2, paragraph 17, the address converter 24 can be any conventional type of solid state memory device, such as a read only memory (ROM), a random access memory (RAM), an electronically erasable programmable read only memory (EEPROM), or the like. It would be obvious to on skilled in the art at the time the invention was made that the memories disclosed above are synchronous in their operation and can not function properly if not clocked and synchronized with Gold's BIST engine 20 and embedded memory 28. The artisan would be motivated to believe so because built-in self-repair circuits inherently adapt the repair circuit to the memory timing it is repairing through synchronization of the signals interfacing to the memory array. In this way the interface circuit of the instant application would already be included in Gold's address converter 24 (mapping circuit). Gold does not explicitly teach "a mapping circuit for each of said plurality of memories", however, Gold does teach the memory address converter 24 (mapping circuit) converts the physical address generated by the BIST engine 20 (controller) to a corresponding logical address in the embedded memory 28 (memory). (Page 2, ¶ 17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to duplicate Gold's address

converter 24 (mapping circuit) and embedded memory 28 (memory) to make *a plurality of memories each having a mapping circuit*, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8 (7th Cir. 1977).

Claims 3 and 10:

Gold teaches the BIST engine 20 (controller) generates the physical memory address 34 (first physical address) and the adjacent physical memory address 36 (second physical address). The BIST engine 20 passes the physical memory address 34 and the physical memory address 36 to the address converter 24 (mapper). The address converter 24 (mapper) maps the physical memory address 34 (first physical address) to the corresponding logical memory address 40 (first logical address), and maps the physical memory address 36 (second physical address) to the corresponding logical memory address 42 (second logical address). The test vectors generated by the BIST engine 20 are then written to the logical memory addresses of the embedded memory array 28. (Page 2, ¶ 23).

Claims 4 and 11:

Gold teaches electronic device 10 includes a BIST engine 20 (self-test controller) that generates a test vector for a physical memory row address of the embedded memory 28 (synthesized memory).

Claim 7:

Gold does not explicitly teach "a plurality of memories, a mapping circuit being provided for each of said memories", however, Gold does teach the memory address

converter 24 (mapping circuit) converts the physical address generated by the BIST engine 20 (controller) to a corresponding logical address in the embedded memory 28 (memory). (Page 2, ¶ 17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to duplicate Gold's address converter 24 (mapping circuit) and embedded memory 28 (memory) to make *a plurality of memories each having a mapping circuit*, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8 (7th Cir. 1977).

11. Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gold (US-2003/0167428) and further in view of Patti (US-6469945).

Claims 2 and 9:

Gold does not explicitly teach the physical address signals include row and column address signals, however, Gold does teach a BIST engine 20 (self-test controller) that generates a test vector for a physical memory row address of the embedded memory 28 (memory). (Page 2, ¶ 17). Gold also teaches the address converter 24 (mapping circuit) may be adapted to support built-in self-repair of the embedded memory array 28. (Page 2, ¶ 21). In addition, Gold suggests the address converter 24 (mapping circuit) can be any conventional type of solid state memory device, such as a read only memory (ROM), a random access memory (RAM), an electronically erasable programmable read only memory (EEPROM), or the like. (Page 2, ¶ 17). Patti teaches that controller 40 loads physical row and column addresses into

row/column address CAM 43 and 42. Patti teaches controller 40 alters the mapping in CAM 43 and 42 when a bad row or column is found such that the bad row or column is replaced by one of the spares. (See col. 4, lines 4-8). Patti's suggests in an analogous art the mapping circuit utilizes a CAM to map the physical address within the memory chip, i.e., rows and columns in the storage array, to the logical addresses, however, the mapping circuit can include some form of non-volatile memory such as EEPROM or FLASH in which the mapping is stored when power is turned off. (See col. 9. lines, 9-18). As previously stated, Gold also teaches the mapping circuit can include an EEPROM or FLASH. (Page 2, ¶ 17). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Gold's BIST engine 20 could be modified with Patti's controller to generate physical column address as well as physical row addresses. Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gold's address converter 24 (mapping circuit) to include a column ROM or EEPROM or FLASH memory as in Patti's mapping circuit. The artisan would be motivated to do so because it would enable Gold to test or replace the memory array 28 columns as well as the rows.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

7/11/05

DAVIDTON
PRIMARY EXAMINER